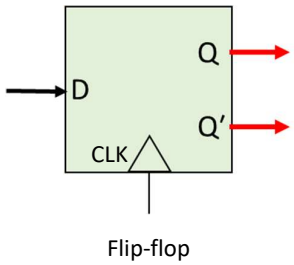
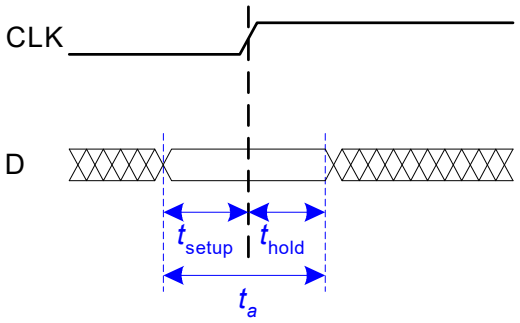
Time constraints for digital circuits

A quick note about the time constraints associated with flip-flops and combinatorial circuits.



Flip-flop

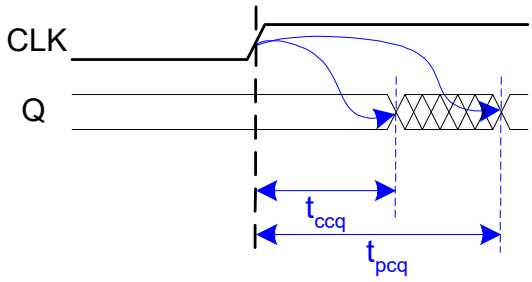


Input constraints for a flip-flop:

- t_{setup} ("Setup Time") is the time **before** the rising edge of the clock CLK during which the **D** input should remain stable (i.e. not changing).
- t_{hold} ("Hold Time") is the time **after** the rising edge of the clock CLK during which the **D** input should not change.
- t_a is the time window where input **D** must be stable ($t_a = t_{setup} + t_{hold}$).

Output constraints for a flip-flop:

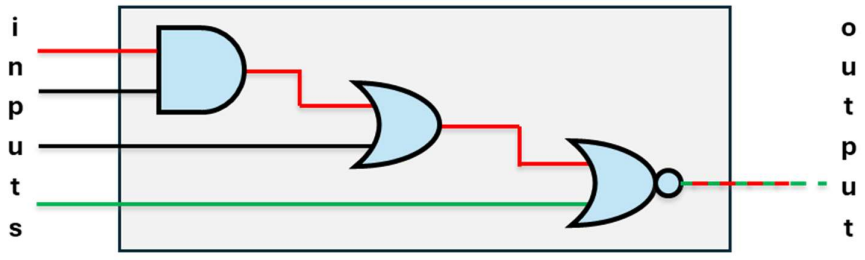
- t_{ccq} ("min CLK to Q delay") is the time **after** the rising edge of CLK at which the **Q** output would be unstable (i.e. could change).
- t_{pcq} ("max CLK to Q delay") is the time **after** the rising edge of CLK at which the **Q** output is guaranteed to be stable.



Minimum and maximum delays for combinatorial circuits:

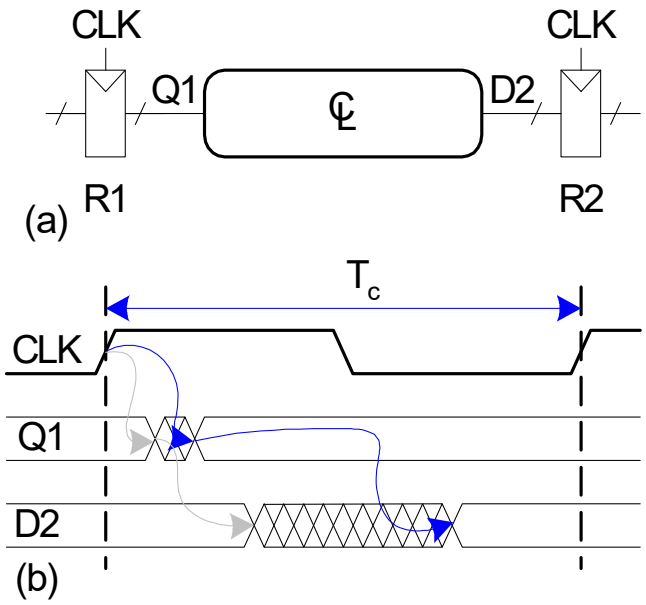
Combinational circuits also have timing constraints for the logic gates. The "min delay" t_{cd} for a circuit (in green) is the minimum time between the moment an input of the circuit changes and the moment the output of that circuit begins to change.

The "max delay" t_{pd} (in red) is the maximum time between when an input to the circuit changes and when the output of that circuit stabilises.



Timing constraints for flip-flops and combinational circuits:

The following diagram shows a circuit for some combinatorial logic between two flip-flops. Here, the input **D2** of flip-flop **R2** comes from the output **Q1** of flip-flop **R1** after passing through the combinatorial circuit **CL.**



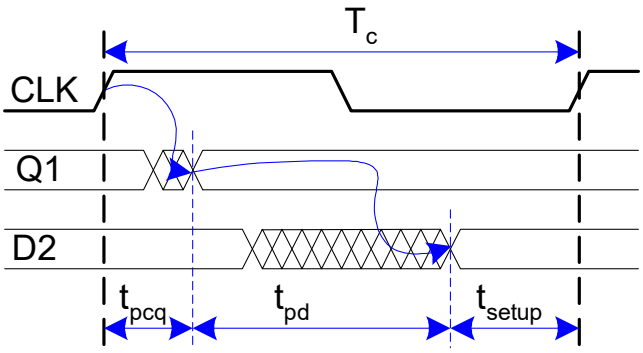
Thus, the output of the **R1_CL** circuit (i.e. **D2**) must be stable for a combined minimum duration greater than or equal to the setup time t_{setup} of the **R2** flip-flop if we want the latter to be able to "see" the new value **D2**. This value must also remain unchanged for a duration t_{hol} after the rising edge of the clock so that the **R2** flip-flop has enough time to make a copy.

To respect the constraint on t_{hold}, we have:

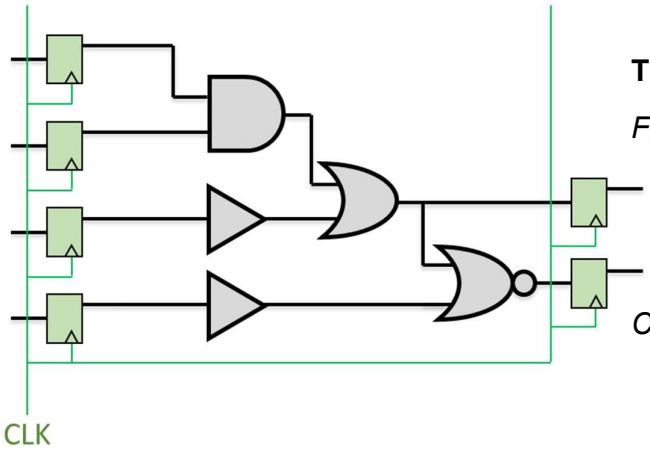
$$\begin{aligned} t_{hold} &< min\_delay(flip\text{–}flop) + min\_delay(CL) \\ &< t_{ccq} + t_{cd} \end{aligned}$$

and to respect the constraint on t_{setup}:

$$\begin{aligned} T_c &\geq max\_delay(flip\text{–}flop) \\ &\quad + max\_delay(CL) \\ &\quad + t_{setup} \\ &\geq t_{pcq} + t_{pd} + t_{setup} \end{aligned}$$



Example:



Timing specifications:

Flip-flops

t_{ccq} = 30 ps, t_{pcq} = 50 ps

t_{setup} = 60 ps, t_{hold} = 70 ps

Combinatorial components

t_{pd} = 35 ps, t_{cd} = 50 ps

t_{pd} circuit = $3 \times 35\ ps = 105\ ps$

t_{cd} circuit = $2 \times 25\ ps = 50\ ps$

Constraint on t_{setup}

$T_c \geq (50 + 105 + 60)\ ps = 215\ ps$
$f_c = 1/T_c \leq 4.65\ GHz$

Constraint on t_{hold}

$t_{ccq} + t_{cd} > t_{hold}$
$(30 + 50)\ ps > 70\ ps$ **verified!**