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### Exercise 1: (10 points)

Consider the following instruction sequence:

- 1: add \$t0, \$t1, \$t2
- 2: sub \$t3, \$t0, \$t4
- 3: lw \$t5, 0(\$t3)
- 4: add \$t6, \$t5, \$t6
- 5: or \$t8, \$t6, \$t5

Assuming a 5-stage MIPS pipeline (IF, ID, EX, MEM, WB), answer the following questions :

1. List all possible data hazards in the code (i.e. affected instructions and registers)

between inst. 1 and 2 (1.rd = 2.rs = \$t0) (2.5 pt. missing details = no mark)  
 between inst. 2 and 3 (2.rd = 3.rs = \$t3)  
 between inst. 3 and 4 (3.rt = 4.rs = \$t5)  
 between inst. 4 and 5 (4.rd = 5.rs = \$t6)  
 between inst. 3 and 5 (3.rt = 5.rt = \$t5)

(0.25 for the correct hazard indication, then 0.25 for the correct registers)

2. if **no forwarding unit is present** (double pumping is available, however) insert in the diagram below the execution stages including where NOPs (i.e. bubbles) occur and indicating double-pumping usage with circles (4.25 pts).

Inst. \ Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
add \$t0, \$t1, \$t2	IF	ID	EX	MEM	WB													
sub \$t3, \$t0, \$t4		IF	nop	nop	ID	EX	MEM	WB										
lw \$t5, 0(\$t3)			nop	Nop	IF	nop	nop	ID	EX	MEM	WB							
add \$t6, \$t5, \$t6						nop	nop	IF	nop	nop	ID	EX	MEM	WB				
or \$t8, \$t6, \$t5									nop	nop	IF	nop	nop	ID	EX	MEM	WB	

3. Now assume a forwarding unit is present (double pumping is still used). Indicate, when applicable, "data forwarding" occurrences with arrows, "pipeline stalls" with "NOP" bubbles, and double-pumping usage with circles (3.25 points)

Inst. \ Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
add \$t0, \$t1, \$t2	IF	ID	EX	MEM	WB													
sub \$t3, \$t0, \$t4		IF	ID	EX	MEM	WB												
lw \$t5, 0(\$t3)			IF	ID	EX	MEM	WB											
add \$t6, \$t5, \$t6				IF	ID	nop	EX	MEM	WB									
or \$t8, \$t6, \$t5				IF	IF	ID	EX	MEM	WB									

## Exercise 2: (10 points)

A processor uses a 2-way set associative data cache with the following parameters:

- Total data size: 16 Kbytes
- Word size: 32 bits (4 bytes per word)
- Memory organization: Byte-addressable
- Block size: 8 words per block
- Replacement policy: Least Recently Used (LRU)
- Physical memory address: 28 bits

Assume at power-up, the entire cache is empty.

1. Show how the main memory address is divided into Tag (T), Index (I), and Block Offset (O) fields.

- 1 block = 8 words  $\times$  4 bytes/word = 32 bytes. **(3 pt. missing details = no mark)**
- Cache size = 16 Kbytes =  $16 (2^4) \times 1024 (2^{10}) = 16384$  bytes.
- Number of lines =  $\frac{16Kb}{32b} = 512$  lines
- 2-way set associative  $\rightarrow$  2 blocks per set
- Total number of sets =  $512/2 = 256$  sets

Step 1: Number of offset bits  

$$\text{Block size} = 32 \text{ bytes} \rightarrow \text{Offset bits} = \log_2 32 = 5 \text{ bits}$$

Step 2: Number of set index bits  

$$\text{set Index bits} = \log_2(256) = 8 \text{ bits}$$

Step 3: Tag bits  

$$\text{Tag bits} = 28 - (8 + 5) = 15 \text{ bits}$$

Address format: Tag(15 bits) | Index(8 bits) | Offset(5 bits)

2. Given the following byte addresses (in hexadecimal) accessed in sequence. For each address complete the table indicating the Tag and set Index bits (in hexadecimal). On the last column, indicate whether it is a cache hit or miss (for a miss, indicate whether it is a compulsory, a conflict or a capacity miss). If a replacement occurred, indicate the Tag of the block evicted (**4 pts missing details = no mark**).

#	Memory Address (Hex)	Tag	Index	Hit/miss
1	0x0A3F420 0000101000111111010000100000	0x51F	0xA1	Compulsory miss (0.25pt)
2	0x0A3F430 0000101000111111010000110000	0x51F	0xA1	Hit
3	0x0A4C890 0000101001001100100010010000	0x526	0x44	Compulsory miss
4	0x2A3F420 0010101000111111010000100000	0x151F	0xA1	Compulsory miss
5	0x0A3F420 0000101000111111010000100000	0x51F	0xA1	Hit
6	0x0A4C8B0 0000101001001100100010110000	0x526	0x45	Compulsory miss

7	0x2A3F421 0010101000111111010000100001	0x151F	0xA1	Hit
8	0x3A3F420 0011101000111111010000100000	0x1D1F	0xA1	Compulsory miss We evict 0x51F

3. What is the overall miss rate?

**0.5pt. missing details = no mark)**

$$\text{Miss rate} = \frac{\text{Number of misses}}{\text{total requests}} = \frac{5}{8} = 62.5\%$$

4. Assume we swap the 2-way associative cache memory described above with a direct-mapped one (i.e. same parameters are used except for the replacement policy which is irrelevant now).

- What happens to *Index* width?
- What happens to *Tag* width?
- How do miss types likely change?

**(1.5 pt. missing details = no mark)**

Same block/line size: no change in the offset field (5 bits).  
Number of lines =  $\frac{16Kb}{32b} = 512$  lines (this time not divided into sets) (0.25pt)

- $index\ bits = \log_2(512) = 9$  bits (the width increases by 1 bit) (0.25pt)
- Tag bits =  $28 - (9 + 5) = 14$  bits (the width decreases by 1 bit) (0.5pt)
- More conflict misses (0.5pt)

5. Now, we reduce the block size to 4 words (16 bytes). The total cache size is the same. How do *Offset*, *Index*, and *Tag* bits change?

**(1 pt. missing details = no mark)**

Offset bits =  $\log_2(16) = 4$  bits (0.25pt)  
Number of lines =  $\frac{16Kb}{16b} = 1024$  lines (0.25pt)  
index bits =  $\log_2(1024) = 10$  bits (0.25pt)  
Tag bits =  $28 - (10 + 4) = 14$  bits (0.25pt)