1. Pre-check

This section is designed as a check to help you determine whether you understand the concepts covered in class. Please answer "true/false" to the following questions and include an explanation.

1.1. The single-cycle datapath uses all hardware units for each instruction.

1.2. Single-cycle datapath stages can be executed in parallel to speed up the execution of a single instruction.

1.3. Combinatorial circuits are only used in the instruction decoding stage.

2. Single-cycle CPU

2.1. In this tutorial, we'll work with the single-cycle datapath shown on the last page.

a) Fill each rounded box with the name of the datapath component and each square box with the name of the control signal.

b) Describe what happens at each step of the datapath.

Instruction Fetch (IF)

Instruction Decode (ID)

EXecute (EX)

MEMory access (**MEM**)

Write**b**ack (**WB**)

2.2. Add the data wires and control signals for the circuit computing the next PC.

2.3. Implement the circuit logic that computes the next PC.

2.4. Fill in the following table with the control signals for the given instructions based on the datapath you completed. In the case where the nature of the control signal does not matter for the instruction under consideration, put an **X** in the corresponding box.

Instrs.	Control signals								
add									
ori									
lw									
sw									
beq									
j									

2.5. **A state circuit** is a component connected to the clock (designated by a triangle at the bottom of the circuit). In order for the component to function correctly, the input signal must be stable before each rising edge of the clock.
The critical path describes the minimum period required for clocking all state elements present in a circuit. The circuit cannot be clocked faster than this period because signal stability is no longer guaranteed for the individual components of the circuit.

For this exercise, assume the duration for each stage in the datapath is as follows (periods are given in picoseconds – 1 ps = 10^{-1} $seconds$):

IF : 200 ps ;   **ID** : 100 ps ;   **EX** : 200 ps ;   **MEM** : 200 ps ;   **WB** : 100 ps

a) For each instruction listed in the table below, indicate with an **X** the datapath stages used and compute the minimum time required for its execution.

	IF	ID	EX	MEM	WB	Total duration
add						
ori						
lw						
sw						
beq						
j						

b) Which instruction(s) exercise the critical path?

c) Based on your previous answer, at what frequency we clock this single-cycle processor?

d) Why single-cycle datapath is inefficient?

e) How can performance be improved? What is the purpose of pipelining?

Instruction Fetch

Instruction Decode

Execute

Memory

WriteBack

Inst[25:21]

Inst[20:16]

Inst[15:11]

Inst[15:0]

Inst[31:26]

Inst[5:0]

Read Addr 1

Read Addr 2

Write Addr

Write Data

Read Data 1

Read Data 2

Write Enable

R[rs]

R[rt]

Sign/Zero extension

Addr

Read Data

Addr

Write Data

Write Enable

Read Data

A

B

Out

Write Data

+4